

# MJ1509 LDMOS TRANSISTOR

Document Number: MJ1509  
Preliminary Datasheet V1.0

## 90W, 28V High Power RF LDMOS FETs

### Description

The MJ1509 is a 90-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

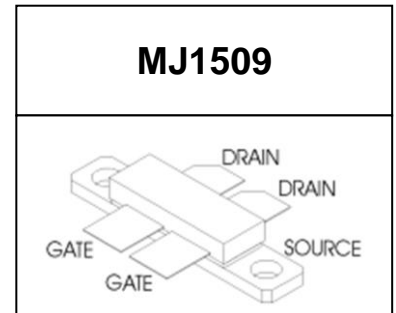
- Typical Performance (on Innogration fixture with device soldered):

$V_{DD} = 28$  Volts,  $I_{DQ} = 500$  mA, CW.

Frequency	Gp (dB)	P <sub>-1dB</sub> (W)	$\eta_D @ P_{-1}$ (%)
1000 MHz	18	90	60

- Typical Performance (on Innogration broadband demo):  $V_{DD} = 24$  Volts,  $I_{DQ} = 600$  mA, CW.

Frequency(MHz)	Pin(dBm)	P <sub>-1dB</sub> (W)	Gp (dB)	$\eta_D @ P_{-1}$ (%)
30	29.40	57.54	18.20	49.33
60	30.10	75.86	18.70	57.36
100	29.00	79.43	20.00	60.18
200	28.30	79.43	20.70	64.02
300	28.00	67.61	20.30	61.78
400	29.30	57.54	18.30	56.28
512	30.20	51.29	16.90	55.50



### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

### Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DS}$	+95	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+40	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

# MJ1509 LDMOS TRANSISTOR

Document Number: MJ1509  
Preliminary Datasheet V1.0

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^{\circ}\text{C}$ , $T_J = 200^{\circ}\text{C}$ , DC test	$R_{\theta JC}$	0.7	$^{\circ}\text{C/W}$

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** ( $T_A = 25^{\circ}\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

**DC Characteristics (per half section)**

Drain-Source Voltage $V_{GS} = 0$ , $I_{DS} = 1.0\text{mA}$	$V_{(BR)DSS}$	95			V
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 75\text{V}$ , $V_{GS} = 0\text{V}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{V}$ , $V_{GS} = 0\text{V}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Gate--Source Leakage Current ( $V_{GS} = 10\text{V}$ , $V_{DS} = 0\text{V}$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$
Gate Threshold Voltage ( $V_{DS} = 28\text{V}$ , $I_D = 150\mu\text{A}$ )	$V_{GS(th)}$	—	2.17	—	V
Gate Quiescent Voltage ( $V_{DD} = 28\text{V}$ , $I_D = 500\text{mA}$ , Measured in Functional Test)	$V_{GS(Q)}$	—	3.3	—	V
Common Source Input Capacitance ( $V_{GS} = 0\text{V}$ , $V_{DS} = 28\text{V}$ , $f = 1\text{MHz}$ )	$C_{ISS}$		TBD		pF
Common Source Output Capacitance ( $V_{GS} = 0\text{V}$ , $V_{DS} = 28\text{V}$ , $f = 1\text{MHz}$ )	$C_{OSS}$		TBD		pF
Common Source Feedback Capacitance ( $V_{GS} = 0\text{V}$ , $V_{DS} = 28\text{V}$ , $f = 1\text{MHz}$ )	$C_{RSS}$		TBD		pF

**Functional Tests** (In Demo Test Fixture, 50 ohm system)  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 500\text{mA}$ ,  $f = 1000\text{MHz}$ , CW Signal Measurements.

Power Gain	$G_p$	—	18	—	dB
Drain Efficiency@P1dB	$\eta_D$	—	60	—	%
1 dB Compression Point	$P_{-1dB}$	—	90	—	W
Input Return Loss	IRL	—	-7	—	dB

**Load Mismatch (In Innogration Test Fixture, 50 ohm system):**  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 600\text{mA}$ ,  $f = 1000\text{MHz}$

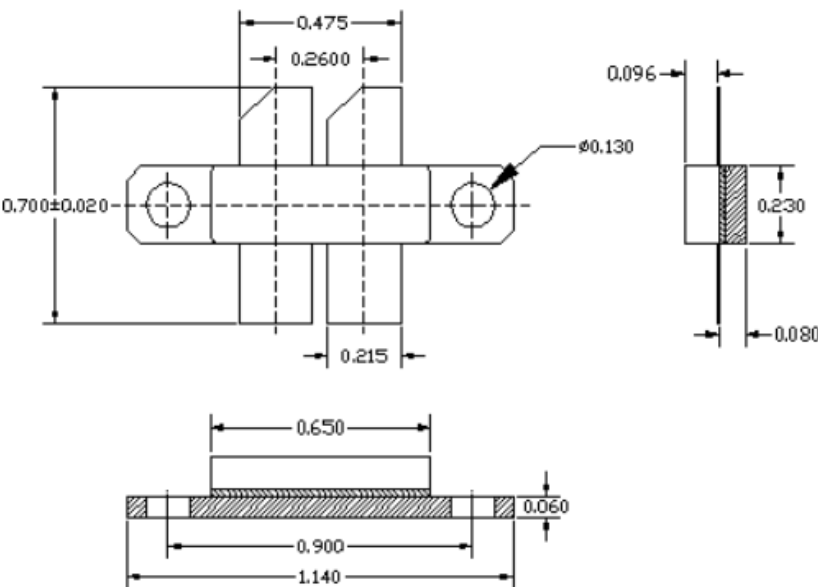
VSWR 20:1 at 90W pulse CW Output Power	No Device Degradation
--	-----------------------

# MJ1509 LDMOS TRANSISTOR

Document Number: MJ1509  
Preliminary Datasheet V1.0

## Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Tolerance .XX +/-0.01 .XXX +/- .005 inches

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-F4E					03/12/2013

# MJ1509 LDMOS TRANSISTOR

Document Number: MJ1509  
Preliminary Datasheet V1.0

## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/05/20	Rev 1.0	Preliminary Datasheet

## Disclaimers

Specifications are subject to change without notice. Innogration believes the information contained within this data sheet to be accurate and reliable. However, no responsibility is assumed by Innogration for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Innogration. Innogration makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose. "Typical" parameters are the average values expected by Innogration in large quantities and are provided for information purposes only. These values can and do vary in different applications and actual performance can vary over time. All operating parameters should be validated by customer's technical experts for each application. Innogration products are not designed, intended or authorized for use as components in applications intended for surgical implant into the body or to support or sustain life, in applications in which the failure of the Innogration product could result in personal injury or death or in applications for planning, construction, maintenance or direct operation of a nuclear facility. For any concerns or questions related to terms or conditions, pls check with Innogration and authorized distributors

Copyright © by Innogration (Suzhou) Co.,Ltd.